HM62V256 Series

32,768-word × 8-bit Low Voltage Operation CMOS Static RAM

HITACHI

ADE-203-136E (Z)
Rev. 5.0
Jun. 19, 1995

Features

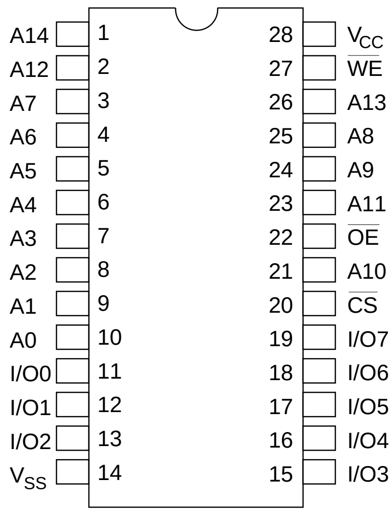
- Low voltage operation SRAM
  Operating Supply Voltage: 2.7 V to 3.6 V
- 0.8 µm Hi-CMOS process
- High speed
  Access time: 70/85/100 ns (max)
- Low power
  Standby: 0.15 µW (typ)
- Completely static memory
  No clock or timing strobe required
- Directly LVTTL compatible: All inputs and outputs

Ordering Information

Type No.	Access Time	Package
HM62V256LFP-10T	100 ns	450 mil 280 pin plastic SOP (FP-28DA)
HM62V256LFP-7SLT HM62V256LFP-10SLT	70 ns 100 ns	
HM62V256LFP-8ULT	85 ns	
HM62V256LT-10	100 ns	8 mm × 14 mm 32 pin TSOP (normal type) (TFP-32DA)
HM62V256LT-8SL	85 ns	
HM62V256LTM-10	100 ns	8 mm × 13.4 mm 28-pin TSOP (normal type) (TFP-28DA)
HM62V256LTM-7SL HM62V256LTM-10SL	70 ns 100 ns	
HM62V256LTM-8UL	85 ns	

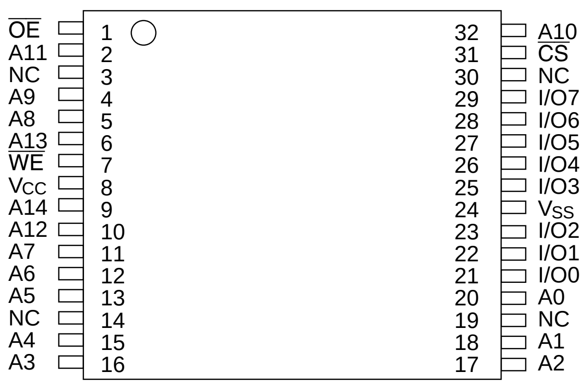
Pin Arrangement

HM62W256LFP Series



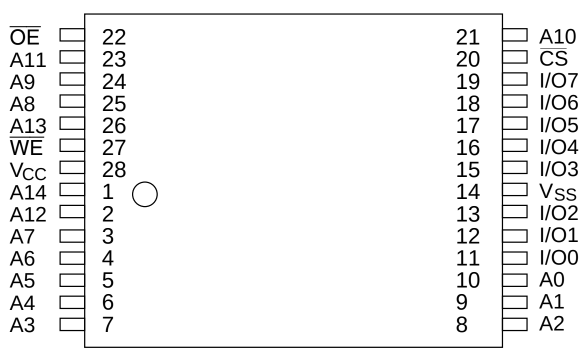
(Top View)

HM62W256LT Series



(Top View)

HM62W256LTM Series

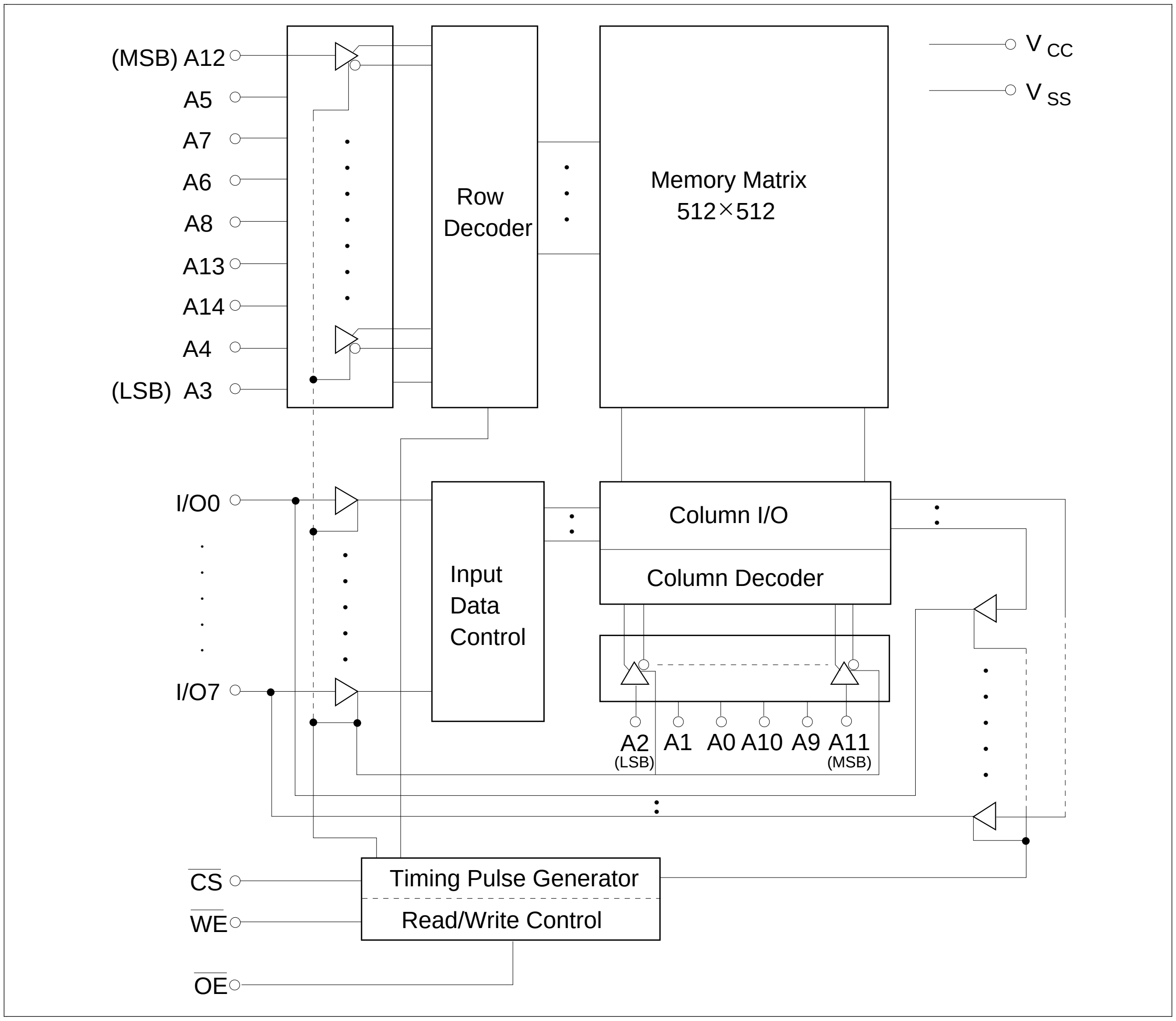


(Top View)

Pin Description

Pin name	Function
A0 to A14	Address inputs
I/O0 to I/O7	Data input/output
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
NC	No connection
V_{CC}	Power supply
V_{SS}	Ground

Block Diagram



Function Table

$\overline{WE}$	$\overline{CS}$	$\overline{OE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
X	H	X	Not selected	I_{SB}, I_{SB1}	High-Z	—
H	L	H	Output disable	I_{CC}	High-Z	—
H	L	L	Read	I_{CC}	Dout	Read cycle (1)–(3)
L	L	H	Write	I_{CC}	Din	Write cycle (1)
L	L	L	Write	I_{CC}	Din	Write cycle (2)

Note: X: H or L

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Power supply voltage*1	V_{CC}	–0.5 to 4.6	V
Terminal voltage*1	V_T	–0.5*2 to V_{CC}+0.5*3	V
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to + 70	°C
Storage temperature	Tstg	–55 to +125	°C
Storage temperature under bias	Tbias	–10 to +85	°C

Notes: 1. Relative to V_{SS}
2. V_T min: –3.0 V for pulse half-width ≤ 50 ns
3. Maximum voltage is 4.6V

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	2.7	3.0	3.6	V
	V_{SS}	0	0	0	V
Input high(logic 1) voltage	V_{IH}	0.7V_{CC}	—	V_{CC}+0.3	V
Input low(logic 0) voltage	V_{IL}	–0.3 *1	—	0.2V_{CC}	V

Note: 1. V_T min: –3.0 V for pulse half-width ≤ 50 ns

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 2.7 V to 3.6V, V_{SS} = 0 V)

Parameter		Symbol	Min	Typ[*1]	Max	Unit	Test conditions
Input leakage current		$\|I_{LI}\|$	—	—	1	µA	$V_{SS} \le Vin \le V_{CC}$
Output leakage current		$\|I_{LO}\|$	—	—	1	µA	$\overline{CS} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$, $V_{SS} \le V_{I/O} \le V_{CC}$
Operating power supply current (DC)		I_{CCDC1}	—	—	15	mA	$\overline{CS} = V_{IL}$, others = V_{IH}/V_{IL} $I_{I/O}$ = 0 mA
		I_{CCDC2}	—	—	10	mA	$\overline{CS} \le 0.2$ V, $V_{IH} \ge V_{CC} - 0.2$ V, $V_{IL} \le 0.2$ V, $I_{I/O}$ = 0 mA
Average operating power supply current	HM62V256-7	I_{CCAC1}	—	—	30	mA	min cycle, duty = 100 %, $I_{I/O}$ = 0 mA $\overline{CS} = V_{IL}$, others = V_{IH}/V_{IL}
	HM62V256-8	I_{CCAC1}	—	—	27		
	HM62V256-10	I_{CCAC1}	—	—	24		
		I_{CCAC2}	—	—	15	mA	Cycle time ≥ 1 µs, duty = 100% $I_{I/O}$ = 0 mA, $\overline{CS} \le 0.2$ V, $V_{IH} \ge V_{CC} - 0.2$ V, $V_{IL} \le 0.2$ V
Standby power supply current		I_{SB}	—	0.1	1	mA	$\overline{CS} = V_{IH}$
		I_{SB1}	—	0.05	50	µA	Vin ≥ 0 V, $\overline{CS} \ge V_{CC} - 0.2$ V,
			—	0.05	10[*2]		
			—	0.05	4[*3]		
Output low voltage		V_{OL}	—	—	0.2	V	I_{OL} = 20 µA
Output high voltage		V_{OH}	V_{CC} – 0.2	—	—	V	I_{OH} = –20 µA

Notes: 1. Typical values are at V_{CC} = 3.0 V, Ta = +25°C and not guaranteed.
2. This characteristic is guaranteed only for L-SL version.
3. This characteristic is guaranteed only for L-UL version.

Capacitance (Ta = 25°C, f = 1.0 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance[*1]	Cin	—	—	5	pF	Vin = 0 V
Input/output capacitance[*1]	$C_{I/O}$	—	—	8	pF	$V_{I/O}$ = 0 V

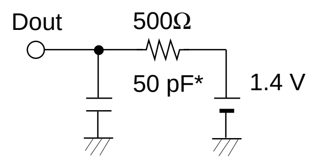
Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 2.7 V to 3.6 V, unless otherwise noted.)

Test Conditions

- Input pulse levels: 0.4 V to 2.4 V
- Input rise and fall time: 5 ns
- Input and output timing reference level: 1.4 V

Output Load



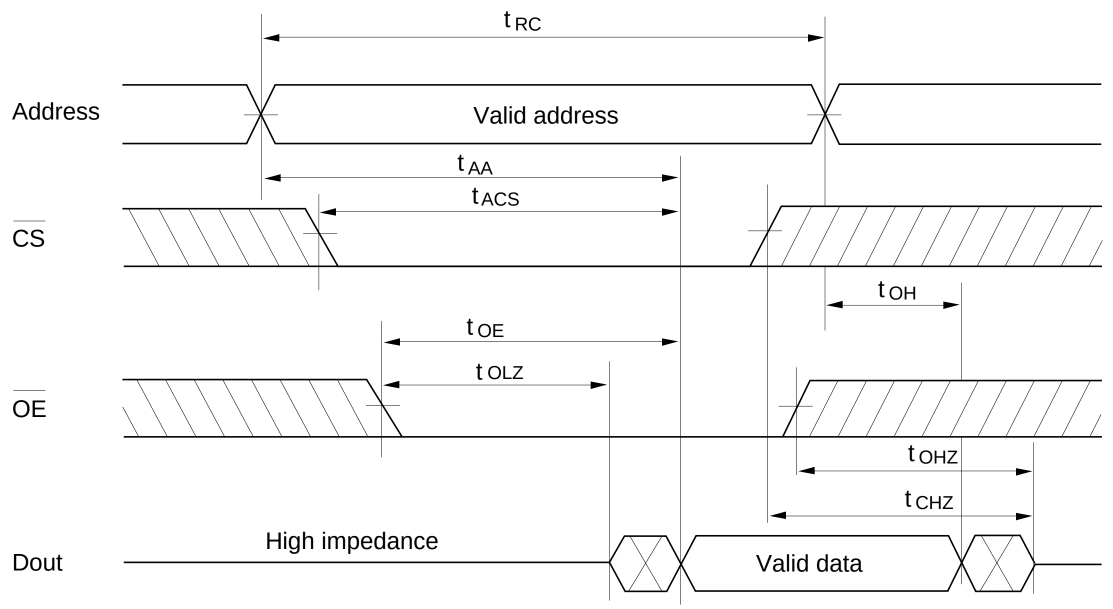
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Read Cycle

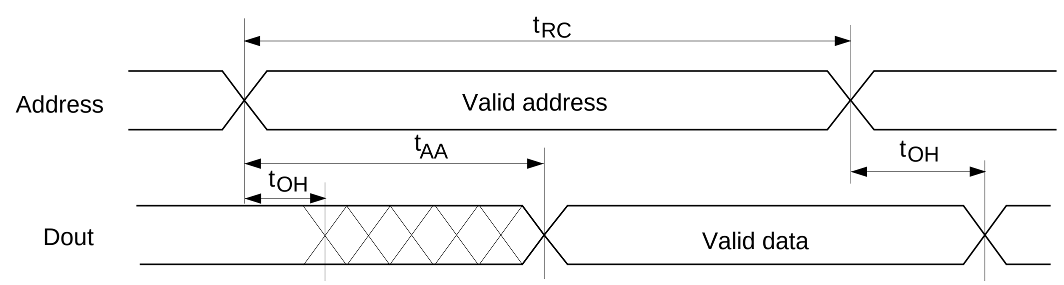
		HM62V256							
		-7		-8		-10			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Read cycle time	t_{RC}	70	—	85	—	100	—	ns	
Address access time	t_{AA}	—	70	—	85	—	100	ns	
Chip select access time	t_{ACS}	—	70	—	85	—	100	ns	
Output enable to output valid	t_{OE}	—	35	—	45	—	50	ns	
Chip selection to output in low-Z	t_{CLZ}	10	—	10	—	10	—	ns	2
Output enable to output in low-Z	t_{OLZ}	5	—	5	—	5	—	ns	2
Chip deselection to output in high-Z	t_{CHZ}	0	25	0	30	0	35	ns	1, 2
Output disable to output in high-Z	t_{OHZ}	0	25	0	30	0	35	ns	1, 2
Output hold from address change	t_{OH}	10	—	10	—	10	—	ns	

Notes: 1. t_{CHZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.
2. This parameter is sampled and not 100% tested.

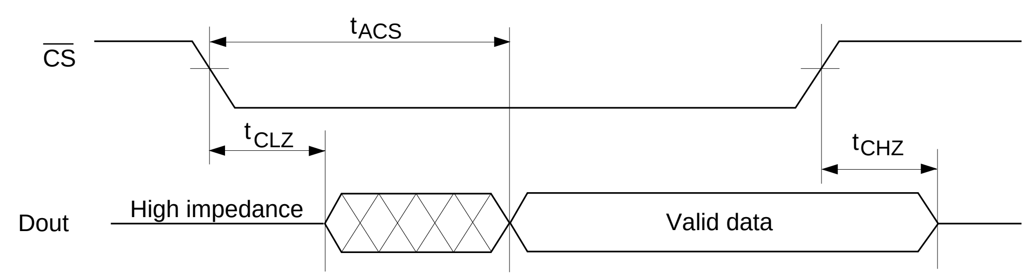
Read Timing Waveform (1) ($\overline{WE}$ = V_{IH})



Read Timing Waveform (2) ($\overline{WE}$ = V_{IH}, $\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IL})



Read Timing Waveform (3) ($\overline{WE}$ = V_{IH}, $\overline{OE}$ = V_{IL})*1



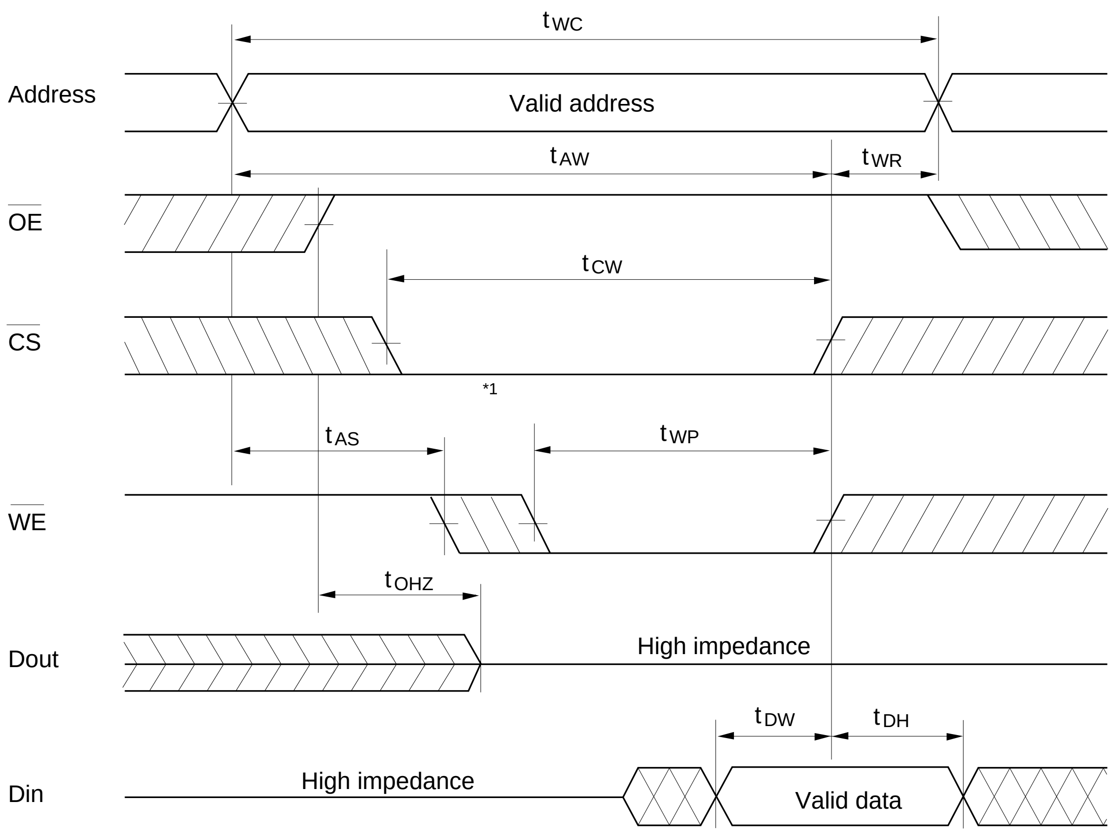
Note: 1. Address must be valid prior to or simultaneously with $\overline{CS}$ going low.

Write Cycle

		HM62V256							
		-7		-8		-10			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Write cycle time	t_{WC}	70	—	85	—	100	—	ns	
Chip selection to end of write	t_{CW}	50	—	75	—	80	—	ns	4
Address setup time	t_{AS}	0	—	0	—	0	—	ns	5
Address valid to end of write	t_{AW}	50	—	75	—	80	—	ns	
Write pulse width	t_{WP}	45	—	55	—	60	—	ns	3, 8
Write recovery time	t_{WR}	0	—	0	—	0	—	ns	6
Write to output in high-Z	t_{WHZ}	0	25	0	30	0	35	ns	1, 2, 7
Data to write time overlap	t_{DW}	30	—	35	—	40	—	ns	
Data hold from write time	t_{DH}	0	—	0	—	0	—	ns	
Output active from end of write	t_{OW}	10	—	10	—	10	—	ns	2
Output disable to output in high-Z	t_{OHZ}	0	25	0	30	0	35	ns	1, 2, 7

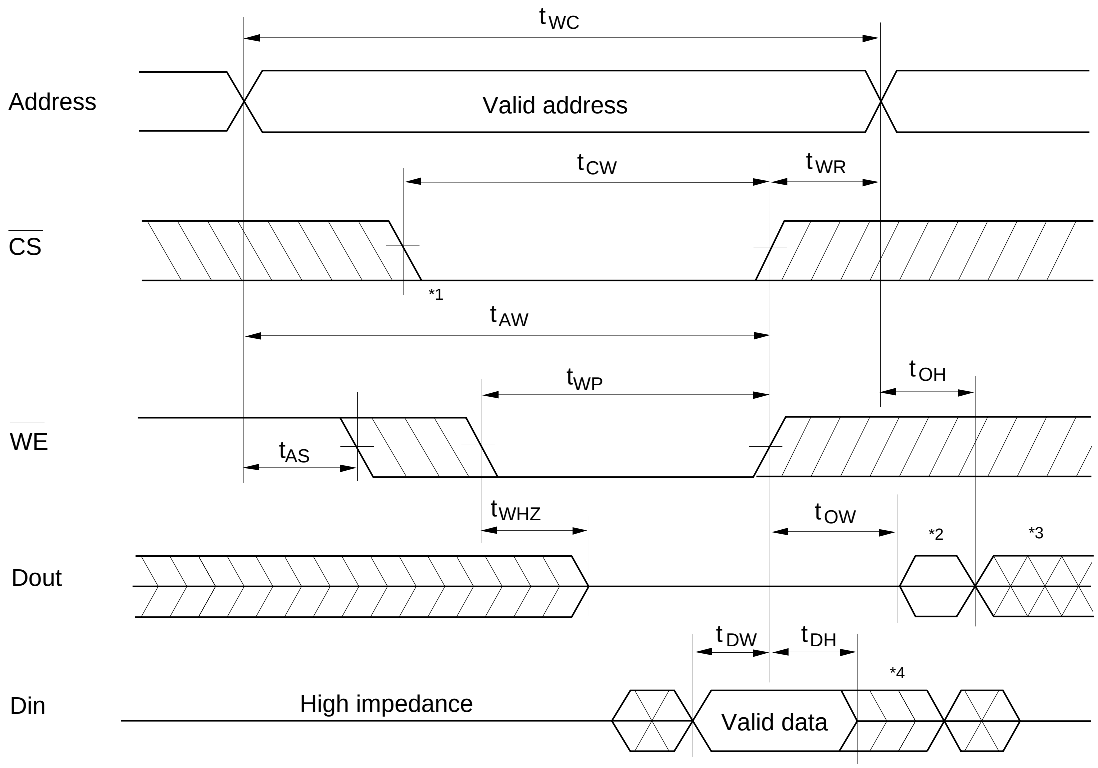
Notes:
1. t_{OHZ} and t_{WHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.
2. This parameter is sampled and not 100% tested.
3. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$. A write begins at the later transition of $\overline{CS}$ going low or $\overline{WE}$ going low. A write ends at the earlier transition of $\overline{CS}$ going high or $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
4. t_{CW} is measured from $\overline{CS}$ going low to the end of write.
5. t_{AS} is measured from the address valid to the beginning of write.
6. t_{WR} is measured from the earlier of $\overline{WE}$ or $\overline{CS}$ going high to the end of write cycle.
7. During this period, I/O pins are in the output state so that the input signals of the opposite phase to the outputs must not be applied.
8. In the write cycle with $\overline{OE}$ low fixed, t_{WP} must satisfy the following equation to avoid a problem of data bus contention, $t_{WP} \geq t_{WHZ}$ max + t_{DW} min.

Write Timing Waveform (1) ($\overline{OE}$ Clock)



Notes: 1. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in the high impedance state.

Write Timing Waveform (2) ($\overline{OE}$ Low Fixed)



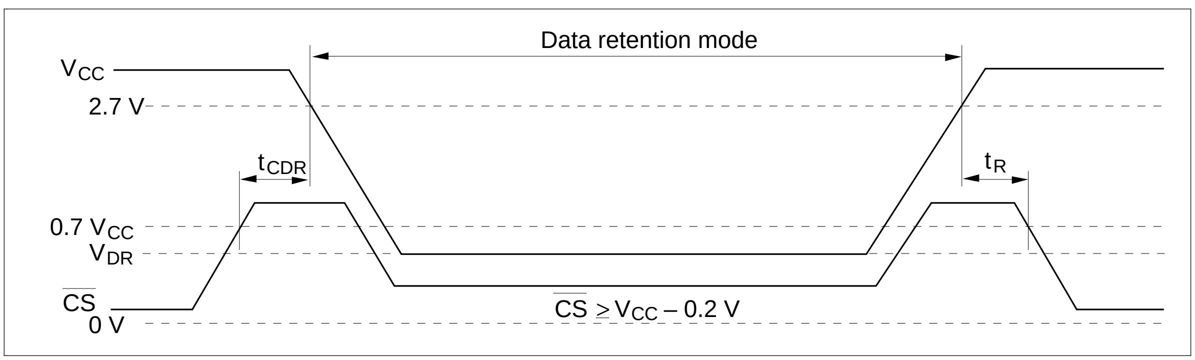
Notes: 1. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in the high impedance state.
2. Dout is the same phase of the write data of this write cycle.
3. Dout is the read data of next address.
4. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Therefore, the input signals of the opposite phase to the output must not be applied to them.

Low V_{CC} Data Retention Characteristics (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ*[1]	Max	Unit	Test conditions*[6]
V_{CC} for data retention	V_{DR}	2.0	—	3.6	V	$\overline{CS} \geq V_{CC} - 0.2$ V, Vin ≥0 V
Data retention current	I_{CCDR}	—	0.05	27*[2]	µA	V_{CC} = 2.7 V, Vin ≥ 0 V $\overline{CS} \geq V_{CC} - 0.2$ V
		—	0.05	7*[3]		
		—	0.05	2*[4]		
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	See retention waveform
Operation recovery time	t_R	t_{RC}*[5]	—	—	ns	

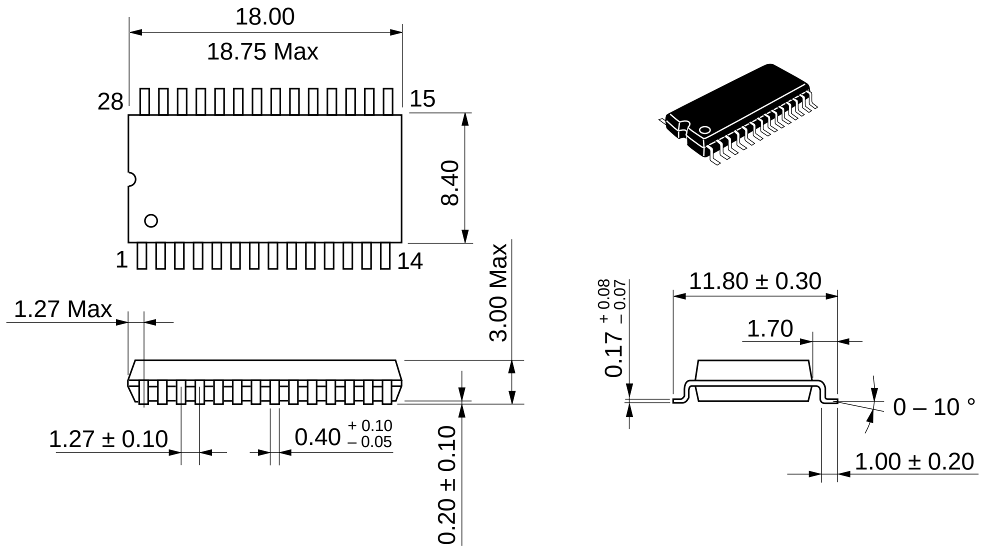
Notes: 1. Typical values are at V_{CC} = 2.7 V, Ta = 25°C and not guaranteed.
2. 9 µA max at Ta = 0 to 40°C.
3. This characteristics guaranteed for only L-SL version. 2.0 µA max at Ta = 0 to 40°C.
4. This characteristics guaranteed for only L-UL version. 0.4 µA max at Ta = 0 to 40°C.
5. t_{RC} = read cycle time.
6. $\overline{CS}$ controls address buffer, $\overline{WE}$ buffer, $\overline{OE}$ buffer, and Din buffer. If $\overline{CS}$ controls data retention mode, other input levels (address, $\overline{WE}$, $\overline{OE}$, I/O) can be in the high impedance state.

Low V_{CC} Data Retention Timing Waveform

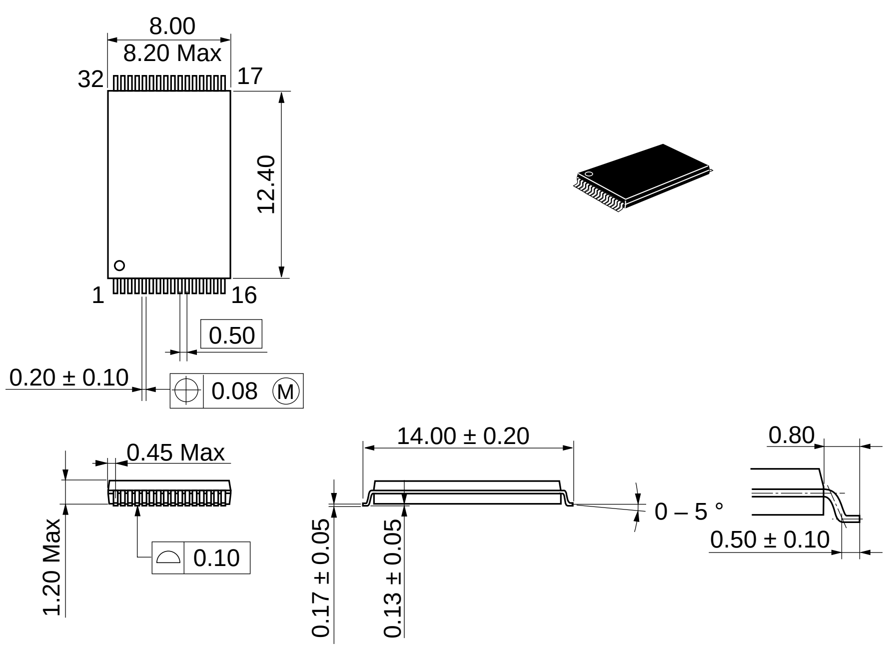


Package Dimensions

HM62V256LFP Series (FP-28DA) Unit: mm



HM62V256LT Series (TFP-32DA) Unit: mm



HM62V256LTM Series (TFP-28DA)

Unit: mm

